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Optimisation of the anodisation processing for aluminium oxide gate dielectrics in ZnO thin film transistors by multivariate analysis

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ABSTRACT

The present study reports a two-level multivariate analysis to optimise the production of anodised aluminium oxide (Al_2O_3) dielectric films for zinc oxide thin-film transistor (TFTs). Fourteen performance parameters were measured and Analysis Of Variance (ANOVA) of the combined responses has been applied to identify how the Al_2O_3 dielectric fabrication process influences the electrical properties of the TFTs. Using this approach, the levels for the manufacturing factors to achieve optimal overall device performance have been identified and ranked. The cross-checked analysis of the TFT performance parameters demonstrated that the appropriate control of the anodisation process can have a higher impact on TFT performance than the use of traditional methods of surface treatment of the dielectric layer. Flexible electronics applications are expected to grow substantially over the next 10 years. Given the complexity and challenges of new flexible electronics components, this 'multivariate' approach could be adopted more widely by the industry to improve the reliability and performance of such devices.

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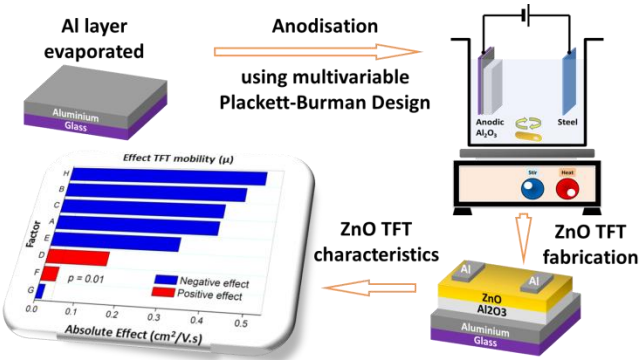


Keywords: design of experiments, Plackett-Burman design, ANOVA, thin-film transistors, aluminium oxide, anodisation.

INTRODUCTION

The global market in flexible displays, solar energy and large area electronics is expected to boom in the next 5-10 years. For example, many market analysts have forecasted the flexible display industry to grow to $30-50bn by 2020 with the rise in next generation e-readers, phone and other flexible displays. Key to realising this potential is the need for flexible, lightweight, transparent, mechanically robust electronics, which has motivated research groups to focus on zinc oxide (ZnO) thin film transistors (TFTs) [1–6]. ZnO can be deposited by using a variety of techniques such as sputtering, chemical vapour deposition, atomic layer deposition and spray coating. The conductivity mechanism of undoped ZnO is still not fully understood, but it is commonly associated to oxygen vacancies, zinc interstitials or substitutional hydrogen impurities [2,3]. Therefore, one key to the performance of ZnO-based TFTs is the control of density of defects [3], which depend strongly on the deposition technique and the quality of gate dielectric layer and the semiconductor/dielectric interface [4].

To improve the performance of ZnO TFTs, there is a need to simultaneously lower the device power consumption, operating voltage, current consumption in the "*off*" state, gate leakage current, improve the threshold voltage stability and the operation frequency [7]. All these factors are critically influenced by the gate dielectric and the semiconductor/dielectric interface properties. To achieve this, the dielectric must concurrently possess i) a large capacitance per unit area, ii) a low leakage current and iii) a low surface roughness to minimize carrier scattering, allowing optimal carrier mobility in the transistor channel during accumulation; and iv) a low interfacial trap density to minimize threshold voltage instabilities [8]. To achieve these qualities, high-κ dielectrics are often used and combined with other materials in a bilayer structure which can be further improved by surface treatment [9,10]. In this context, Al_2O_3 has been considered a promising dielectric due to its

high dielectric constant (7.5 to 15) and high thermal stability. Whilst Al_2O_3 has been deposited using magnetron sputtering [11], chemical vapor deposition (CVD), atomic layer deposition (ALD) [12], the anodisation process is particularly interesting for flexible electronics owing to its simplicity, low cost, low temperature, potential for R2R development and excellent film thickness control in nanometric scale [13]. Furthermore, the electrical properties of anodised films are shown to be better when compared with other techniques [14,15].

To develop anodised layers, there are several factors that impact the electrical and morphological properties of the film. Ordinarily, these are studied by varying each factor individually, with all other factors being kept constant. This can be a slow and inefficient method for elucidating the main factors that affect the performance of a TFT. To avoid this, a "design of experiments" (DOE)[16,17] approach can be applied to screen the main factors and identify which have the greatest significance on the device response whilst using a reduced number of runs.

In this work, a comprehensive study of the influence of the processing parameters on the performance of anodised Al_2O_3 insulating films for ZnO TFTs built is conducted. In particular, a combinational science approach is undertaken in order to provide a rapid methodology to optimise the layer deposition. This approach could provide a step-change for process optimisation for researchers in the area of flexible electronics. To accomplish this, a screening of the anodisation parameters was carry out by using a Plackett-Burman Design (PBD)[18–21] which enables several parameters to be varied simultaneously, with reduced number of experiments, providing an efficient and rapid method to identify the most significant factors which impact the TFT performance. We studied eight different process parameters that influence the performance parameters of ZnO TFTs (mobility, threshold voltage, etc.) by using analysis of variance

(ANOVA)[22–24]. In our view, this procedure could be adopted more widely in flexible electronics development to increase the speed of product development.

EXPERIMENTAL DETAILS

Device fabrication steps

All steps of fabrication, including anodisation and sputtering, were carried out in the cleanroom class 1000. Substrates were thoroughly cleaned with solvents and oxygen plasma treated for 5 minutes. Eight different factors with two levels considered for the anodisation process are listed in table 1. Values on table 1 are the average of 4 to 7 measurements and the uncertainty is given by the corresponding standard deviation, except by the final voltage (H) and the current density (F), which were determined by the accuracy of the voltage/current source unit (Keithley SMU model 237). Details on the anodisation process are presented in the supporting information material (SI).

Aluminium films were evaporated onto glass substrates using a Leybold 250 Univex thermal evaporator and anodisation process was carried out according to factors and levels given in table 1. The thickness (t) of the Al_2O_3 films were determined by the final voltage (V_F) of the anodisation process from the relationship, $t = cV_F$, being c a constant factor which depends on the experimental conditions (considered as ~ 1.2 nm/V in this work) [14,15]. After anodisation, the films were removed from the solution and the impact of post annealing considered; samples were either left to dry at room temperature or annealed at 150ºC for 1 hour.

Table 1: Factors chosen for using in the screening test of the two-level factorial factors by the PBD and correspondent values.

	Factors	Unit	Low value	High value
A	Thickness of Al-layer	nm	60.7 ± 1.3	201.2 ± 1.4
B	Al evaporation rate	Å /s	5.1 ± 0.5	15.0 ± 0.6
C	H_2O content	%	16 ± 0.5	30 ± 0.5
D	Temperature of electrolyte	C	40.8 ± 1.1	60.1 ± 1.3
E	pH of the electrolytic solution	-	6.04 ± 0.22	5.07 ± 0.0.21
F	Current density	mA/cm^2	0.45 ± 0.001	0.65 ± 0.001
G	Annealing	ºC	Without thermal treatment	Annealed at 150 ºC
H	Final voltage	V	30.0 ± 0.01	40.0 ± 0.01

The performance of the Al_2O_3 films as a dielectric layer was tested manufacturing metal-insulator-metal (MIM) capacitor structures and bottom-gate/top-contact ZnO TFTs. For TFTs, ZnO films were deposited onto the Al_2O_3 film by the Leybold 350 Univex sputter coating system. The pressure of the Ar gas was kept at $1.2x10^{-2}$ Torr, with the power set at 75 W. The thickness (40nm) as well as the evaporation rate (0.5 Å/s) of the ZnO films were controlled by a quartz crystal sensor. To complete the transistors or the MIM capacitors, a top layer of aluminium (70 nm thick) was thermally evaporated through a shadow mask to form a circular electrode, which has a central electrode with 1 mm of diameter surrounded by a concentric ring, with a 400 µm gap (W = 6280 µm and L = 400 µm). For transistor devices, the inner electrode and the external ring were, respectively, the drain and source electrodes, with the Al layer underneath the Al_2O_3 layer contacted as the gate electrode, whereas, for the MIM capacitor configuration, the external ring was grounded, working as a guard ring. The guard ring configuration avoids errors which can occur when performing impedance/capacitance measurements in MIM/MIS capacitor structures since lateral currents may result in charging of the whole gate electrode, misleading the correct evaluation of the device area [25]. For TFT measurements, the external ring does not perform the role of guard ring, acting merely as the transistor drain (or source) electrode.

Characterization setups

The electrical performance of both types of devices (ZnO TFTs and Al_2O_3 MIM capacitors) were evaluated for each test run. Fourteen parameters were used for the analysis, which were separated in three different groups: i) parameters for evaluation of the Al_2O_3 oxide film, obtained from impedance/capacitance spectroscopy measurements in MIM capacitors and AFM images; ii) parameters obtained from the TFT characteristic curves, associated to the carrier transport in the semiconducting film or at the semiconductor/dielectric interface; and iii) parameters obtained from the source-to-gate current curves, focusing on the quality of the dielectric layer during a TFT measurement.

The first group includes the Al_2O_3 dielectric constant (ε), the ac conductivity at low frequencies (σ_{LF}) and the ac conductivity at high frequencies (σ_{HF}). As an additional response parameter of the dielectric film quality, we considered the root mean square (RMS) roughness of the anodised surface, determined from atomic force microscopy (AFM) images.

The second group comprises the ZnO TFT electron mobility (μ), the threshold voltage (V_{th}), the hysteresis of the transfer curve (ΔV_H), the "*off*" state current (I_{off}), the "*on*" state current (I_{on}) and the on/off ratio (I_{on}/I_{off}).

The third group used as response parameters the gate current in the depletion state (I_{dep}), the gate current in the accumulation state (I_{acc}), the voltage of minimal gate current in forward scan (V_{for}) and the voltage of minimal gate current in reverse scan (V_{rev}). In this paper, we focus on the response parameters from the second group, which are more important to the TFT performance. The results for the first and third group are available in the supplementary information (SI).

All the electrical measurements were performed at room conditions, avoiding exposure to ambient light, since ZnO presents persistent photoconductivity when irradiated by UV-light [26,27].

For the TFT measurements, a two-channel source-measure unit (SMU, Agilent model B2902A) was used, with spring probe connectors to perform the contacts to the electrodes (drain, source and gate) and a voltage sweep ratio of 0.5 V/s for both V_{DS} and V_g. Impedance/capacitance measurements were performed by a HP precision LCR meter (model 4282A), using a ac voltage of 100 mV_{RMS} and a frequency range from 20 Hz up to 1 MHz. The atomic force microscopy (AFM) data were obtained by using a Veeco NanoMan system.

Design of experiments (DOE)

The design of experiments used for screening the anodisation factors introduced in Table 1 is based on a matrix sequence of the twelve runs according a Plackett-Burman design (PBD) presented in Table 2. Plackett-Burman Design (PBD) is a screening test of 2-levels fractional factorial design applied to study N-1 variables using N experimental runs, where N is a multiple of four [18]. The table used for this experiment was sourced from Esbensen, K. H. *et al* [28]. In Table 2, the letter L and H refers to the "low value" and "high value" for each process factor, respectively, whereas the letters A to H refers to the anodisation factors, which are specified in Table 1. For each experimental run, a set of measurements (TFT curves, ac impedance or AFM) was carried out on eight replicated samples used for each run. It is worth to mention that the combination of experimental runs and their respective low and high levels of the factors specified in Table 2 were determined in a way that is possible to apply ANOVA for screening the most significant ones. Moreover, another characteristic of the PBD matrix in Table 2 is its orthogonality, i.e., for each level (high or low) in one factor, there is an even number of "highs" and "lows" for all the remaining factors of the matrix.

Table 2: Plackett-Burman matrix for 12 runs experiments screening eight factors (A-H).

Run	A	B	C	D	E	F	G	H
1	L	L	L	L	L	L	L	L
2	H	L	H	H	L	H	H	H
3	L	L	L	H	L	H	H	L
4	H	L	L	L	H	L	H	H
5	H	H	L	H	H	H	L	L
6	L	H	L	H	H	L	H	H
7	H	H	H	L	L	L	H	L
8	L	L	H	L	H	H	L	H
9	H	L	H	H	H	L	L	L
10	H	H	L	L	L	H	L	H
11	L	H	H	L	H	H	H	L
12	L	H	H	H	L	L	L	H

Analysis of Variance (ANOVA)

ANOVA (Analysis Of Variance) has been used to identify which processing condition of the dielectric layer contributes more significantly to a determined best TFT response parameter (e.g. μ, V_{th}, I_{on}, I_{off}, ΔV_H, I_{dep}) [29]. As ZnO TFTs possess sample-to-sample variability, it is vital to consider this variation compared to the variation achieved by changing one or more process conditions. The effect of a factor on a response parameter is defined as:

$$Ef = \frac{\sum Y_+}{n_+} - \frac{\sum Y_-}{n_-} \quad (1)$$

where $\sum Y_+$ is the sum of the response parameter at the high level, $\sum Y_-$ is the sum of the response parameter at the low level and n_+ and n_- are, respectively, the number of experiments in the "high" and "low" levels. The total sum of squares (SS_T) [16] is defined as:

$$SS_T = \frac{N}{4}(Ef)^2 \quad (2)$$

which can be split into two contributions: the sum of squares of the regression (SS_R) and the sum of squares of the error (SS_E). The former is determined by the sum of squares of the effects caused by changing the process conditions ('between-run variation') whereas the latter is

determined by the effects considering devices fabricated by the same process conditions ('within-run variation'). The mean square of regression (MS_R) and the mean square of errors (MS_E), are given by:

$$MS_R = \frac{SS_R}{df_R} \qquad \text{and} \qquad MS_E = \frac{SS_E}{df_E} \tag{3}$$

where df_R and df_E are the degrees of freedom of the regression and the error, respectively. For MS_R, the degrees of freedom are the total number of groups ('test runs') minus one (12 – 1 = 11). For MS_E, the degrees of freedom are the total samples used for these tests minus the groups (96 – 12 = 84).

To perform ANOVA analysis, the ratio between MS_R and MS_E ('the *F*-ratio') is used to test the following two hypotheses [16]:

$$F = \frac{MS_R}{MS_E} \tag{4}$$

- *H0*: *There is no difference between the variance caused by changing the process condition (e.g. pH, current density, temperature of the electrolyte) and the variance caused by noise*.
- *H1*: *The variance caused by stress factor (e.g. pH, current density, temperature of the electrolyte) is larger than the variance caused by noise.*

Under the null hypothesis, the ratio follows the *F* distribution with degrees of freedom of *11* and *84*. Finally, the *p*-value is computed from the *F*-ratio, and this can be used to calculate the difference between the variance caused by the corresponding change on the process condition and the variance caused by noise.

By applying ANOVA to the TFT performance data, a variance table can be calculated. The *p*-value for each process condition can be calculated and a hypothesis test for significance applied. For this work, a significance level α of 0.01 was used to compare with the *p*-values. A small *p*-

value (typically ≤ 0.05) indicates compelling evidence against the null hypothesis, thus leading to the rejection of the null hypothesis. In this work, we used Chemoface, which is a free user-friendly interface developed by the Federal University of Lavras (UFLA), Brazil [21], to perform the factor screening by ANOVA.

RESULTS AND DISCUSSION

Transistor characteristics

To analyse the results TFT performance parameters were extracted from each test run, which were used as output responses for the Plackett-Burman design. Figure 1-a and 1-b show, respectively, the output and transfer curves for a TFT manufactured using Test Run 3 from Table 2. Figure 1-b inset shows a cross-section schematic of the TFT structure used for this work. The $I_D^{\frac{1}{2}}$ vs. V_G curve is also depicted in Fig. 1-b, allowing the evaluation of the TFT mobility (μ) from the slope of the curve and the threshold voltage (V_{th}) from the extrapolation of the linear region to the horizontal axis. In the saturation region, the relationship between the channel current (I_D) and the gate voltage is given by [29]:

$$I_D = \frac{wC_i}{L}\mu\frac{(V_G - V_{th})^2}{2} \quad (5)$$

where w is the channel width, L, the channel length, and C_i, the dielectric layer capacitance per unit area. From the transfer curves for run 3, a mobility of 1.27 cm^2/s, an on/off ratio of 1.4 $x10^4$ and a threshold voltage of 3.5 V were obtained. The performance parameters "on" current, "off" current

and on/off ratio were defined as the maximum channel current in accumulation, the lowest channel current in depletion, and their ratio, respectively.

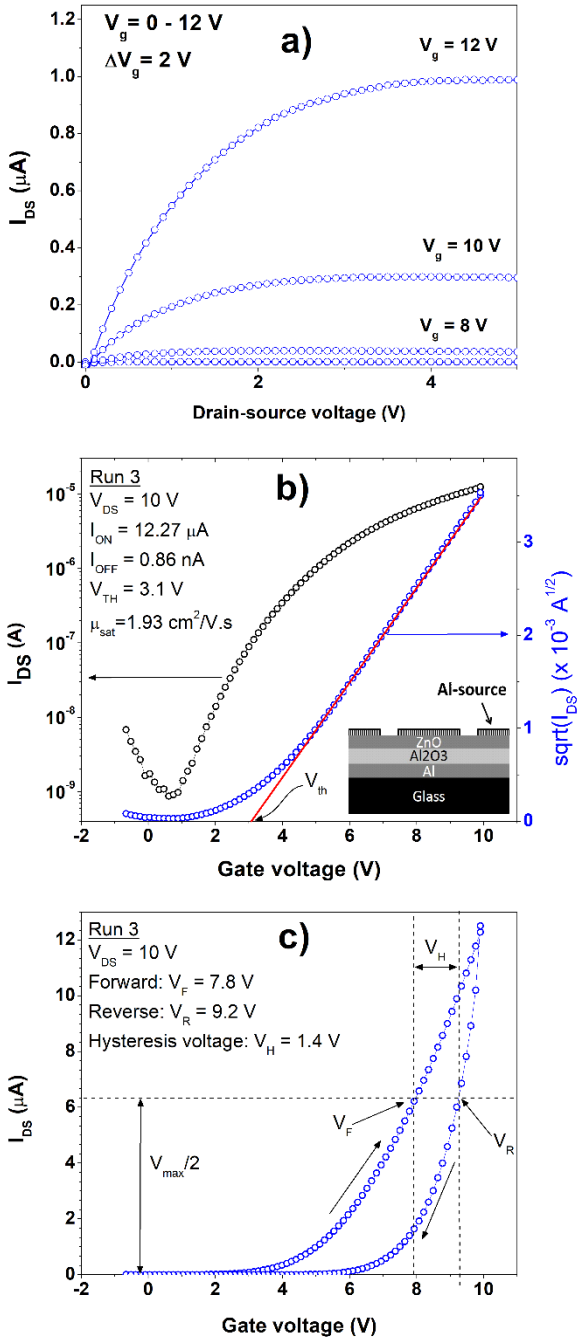


Figure 1: a) Output curves sweeping V_G from 0 to 12 V, in of 2 V steps; b) transfer curve and $I_D^{1/2}$ vs. V_G for V_{DS} = +10 V. Inset: schematic of the ZnO TFT structure; c) transfer curve, for V_{DS}=10 V, showing the hysteresis between forward and reverse voltage scan; All curves were obtained from a ZnO TFT with anodised Al_2O_3 prepared as specified in run # 3, Table 2

The TFT transfer curves normally showed hysteresis on the channel current (I_D) when the voltage at the gate electrode (V_G) was swept in forward or in reverse direction. The evaluation of the hysteresis was undertaken using the method reported elsewhere [30], in which the hysteresis magnitude (ΔV_H) is defined as the voltage difference in the transfer curves, between forward and reverse scan, when the channel current is half of its maximum value. In Figure 1-c, the transfer curve (in linear scale, to highlight the hysteresis) shows clearly the hysteresis for a device constructed in accordance with Run 3 (where ΔV_H = 1.5 V).

Aluminium oxide produced by aqueous combustion synthesis as the dielectric layer [31,32] are also an alternative to obtain high performance TFTs using simple, solution-processed deposition techniques. Despite the excellent quality of the dielectric layer obtained by this technique, annealing temperatures in the order of 350 ^{o}C are still necessary to obtain good insulating films, limiting to a certain extent the use of flexible substrates. Anodisation process, on the other hand, permits the use of relatively low temperatures which are totally compatible to flexible substrates (the substrates were submitted to temperatures ranging from 40^{o}C up to 150^{o}C in the present work).

Influence of the dielectric layer fabrication factors on the ZnO TFTs characteristics

To study how variations in the dielectric layer manufacturing process affect the TFT characteristics, we analysed the characterization parameters (μ, V_{th}, ΔV_H, I_{on}, I_{off} *and* I_{on}/I_{off}) from TFTs which were built using the same ZnO layer process conditions and different dielectric layers fabricated according to the PBD defined by Tables 1 and 2.

The mean values ($\overline{Y}_n$) and the standard deviation values (s_n) of the TFT response parameters (each run has an average of 8 devices) are presented in Table 3. By default, the transfer curve was obtained by repeating the measurement three times, with no visible change (other than the

hysteresis) from one cycle to the next. The mean value from all experiments (between-runs) for a particular response is denoted by $\overline{Y_T}$ whereas s_T is the correspondent between-runs standard deviation (SD) of the within-run means. Moreover, $\bar{s}_n$ is the mean of the within-run standard deviation.

Table 3: Mean and standard deviation values of response parameters from the performance of ZnO TFT onto anodised Al_2O_3 for the 12 experimental runs using PBD method.

Run	μ ($cm^2.V^{-1}.s^{-1}$)		V_{TH} (V)		I_{ON} (μA)		I_{OFF} (nA)		I_{ON}/I_{OFF} ($x10^3$)		ΔV_H (V)	
	$\overline{Y_n}$	s_n	$\overline{Y_n}$	s_n	$\overline{Y_n}$	s_n	$\overline{Y_n}$	s_n	$\overline{Y_n}$	s_n	$\overline{Y_n}$	s_n
1	1.30	0.11	4.09	0.65	4.31	1.13	5.58	0.77	0.76	0.14	3.54	0.58
2	0.15	0.02	0.31	1.00	1.97	0.77	0.48	0.21	4.73	2.96	3.50	0.56
3	1.59	0.17	3.99	0.64	3.44	0.64	1.82	0.61	2.09	0.75	2.05	0.33
4	0.11	0.06	3.90	0.96	2.90	0.74	0.27	0.12	12.83	6.39	1.93	0.41
5	0.33	0.06	2.90	0.67	3.52	0.63	0.66	0.25	6.53	3.99	2.17	0.41
6	0.21	0.06	3.26	0.88	3.08	0.46	0.48	0.19	7.51	3.69	2.58	0.38
7	0.09	0.05	2.63	0.82	0.49	0.30	0.42	0.10	1.15	0.56	4.10	0.35
8	0.19	0.02	2.66	0.58	0.57	0.14	0.26	0.10	2.63	1.41	4.44	0.72
9	0.39	0.04	2.73	0.58	2.07	0.35	0.36	0.13	6.44	2.49	2.34	0.37
10	0.06	0.03	3.06	1.02	0.34	0.11	0.26	0.12	1.80	1.51	4.74	0.54
11	0.15	0.02	4.53	1.00	0.48	0.15	0.41	0.14	1.27	0.50	1.31	0.29
12	0.14	0.02	3.46	1.23	0.42	0.11	0.58	0.24	0.83	0.34	6.05	0.55
$\overline{Y_T}$	0.39		3.13		1.97		0.97		4.05		3.23	
s_T	0.50		1.09		1.46		1.51		3.69		1.41	
$\bar{s}_n$		0.06		0.84		0.40		0.17		1.46		0.41

From Table 3, it is possible to qualitatively estimate the influence of the variation on the factors from the comparison of the between-run standard deviation (s_T) to the mean of the in-run standard deviation ($\bar{s}_n$). The value of the between-run standard deviation compared to the total mean of the response also suggests that the manufacturing factors influence the observed response parameters. For instance, focusing on the TFT mobility, the between-runs SD (0.50 $cm^2.V^{-1}.s^{-1}$) is even higher than the total mean value (0.39 $cm^2.V^{-1}.s^{-1}$), and several times higher than the mean in-run SD ($\bar{s}_n$ = 0.06 $cm^2.V^{-1}.s^{-1}$), indicating that factor variation has strong influence on the TFT mobility.

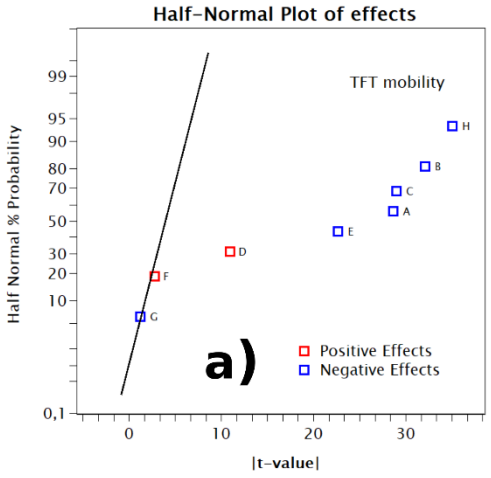
To understand if the manufacturing factors have a statistically significant impact upon the quality of the dielectric layer, ANOVA calculations were performed considering the response parameters obtained from all samples in all experimental run. The calculated effects from all sources of variation (factors) on the TFT mobility, the sum of squares and the percentage of contribution are presented in Figure 2-b. The corresponding half-normal plot for the absolute effects is also shown in Figure 2-a. The half-normal plot highlights that the factors H, B, C, A, E and D do not follow the normal distribution, considering a confidence interval of 99% (*p*-limit of 0.01). For the considered number of degrees of freedom and confidence interval, the *t*-value (defined as the square root of the *F*-ratio from equation 1) limit is 2.642. The vertical axis of Fig. 2-a is in "probability scale", which represents the inverse of a cumulative Gaussian distribution, *i.e. Y' = norminv(Y/100).* The function *norminv*(x_p) computes the deviate x_p associated with the given lower tail probability *p* (0.01, in the present case) of the standardized normal distribution. x_p is calculated for the given *p* such that:

$$p = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x_p} e^{-u^2/2}\, du \qquad for -\infty < x_p < \infty \tag{6}$$

Therefore, the cumulative Gaussian distribution is represented by the straight line of Fig. 2-a. Factors distancing the cumulative Gaussian distribution contribute to the rejection of the null hypothesis (H_0).

Figure 2-b shows the ranking of the factors considering the effect on the TFT mobility. Six factors (H, B, C, A, E and D) are significant within the confidence interval. However, as a convention, we decided to consider as relevant only factors whose contribution to the effect is superior to the fraction correspondent to a uniform distribution among all the 8 factors (i.e., superior to 12.5%). This criterion was used to discriminate the factors which contribute more to the effect from factors, which, even though are significant, contribute less to the observed effect. Factors F

and G were found to be non-significant, which means that the calculated effect of these parameters on the mobility could not be distinguished from noise. The factors which contribute most to the TFT mobility are (in rank order): the final voltage for the anodisation process, the Al-evaporation rate, the electrolyte water content, and the thickness of the Al layer. All these factors presented a negative effect on the mobility, which means that when the factor is set on the "high" value (Table 1), a decrease on the TFT mobility was observed.



Response: TFT mobility							
Factor	Effect	Sum of squares	F-value	p-value	significant	Contribution (%)	Cumulative contribution (%)
H	-0.50	0.250	1218.8	< 0.001	yes	26.93	26.93
B	-0.46	0.210	1024.3	< 0.001	yes	22.63	49.56
C	-0.41	0.172	834.8	< 0.001	yes	18.45	68.01
A	-0.41	0.167	813.1	< 0.001	yes	17.97	85.98
E	-0.32	0.104	507.5	< 0.001	yes	11.21	97.19
D	0.16	0.024	118.2	< 0.001	yes	2.61	99.81
F	0.04	0.002	7.5	0.0077	no	0.16	99.97
G	-0.02	0.000	1.4	0.2482	no	0.03	100.00

Factors Labels:
A: Thickness of Al-layer
B: Al-evaporation rate
C: Water content
D: Temperature of electrolyte
E: pH of the electrolyte
F: Current density
G: Annealing
H: Final voltage

b)

Figure 2: a) Half Normal Plot of effects using the TFT mobility as the response parameter. b) Ranking of the factor effects considering the as TFT mobility response parameter. Corresponding sum of squares of the effects, F-value, p-value, significance, percental contribution and cumulative contribution of each factor on the effects are also computed on the table.

To discriminate the effects by varying the different manufacturing factors, we performed ANOVA on all the results, leading to the Pareto charts of effects presented in Fig. 3. In these charts, the most significant factors are ranked and the threshold limit of significance (p = 0.01) is represented by a vertical dashed line. A factor which absolute effect surpass the p-limit are considered significant.

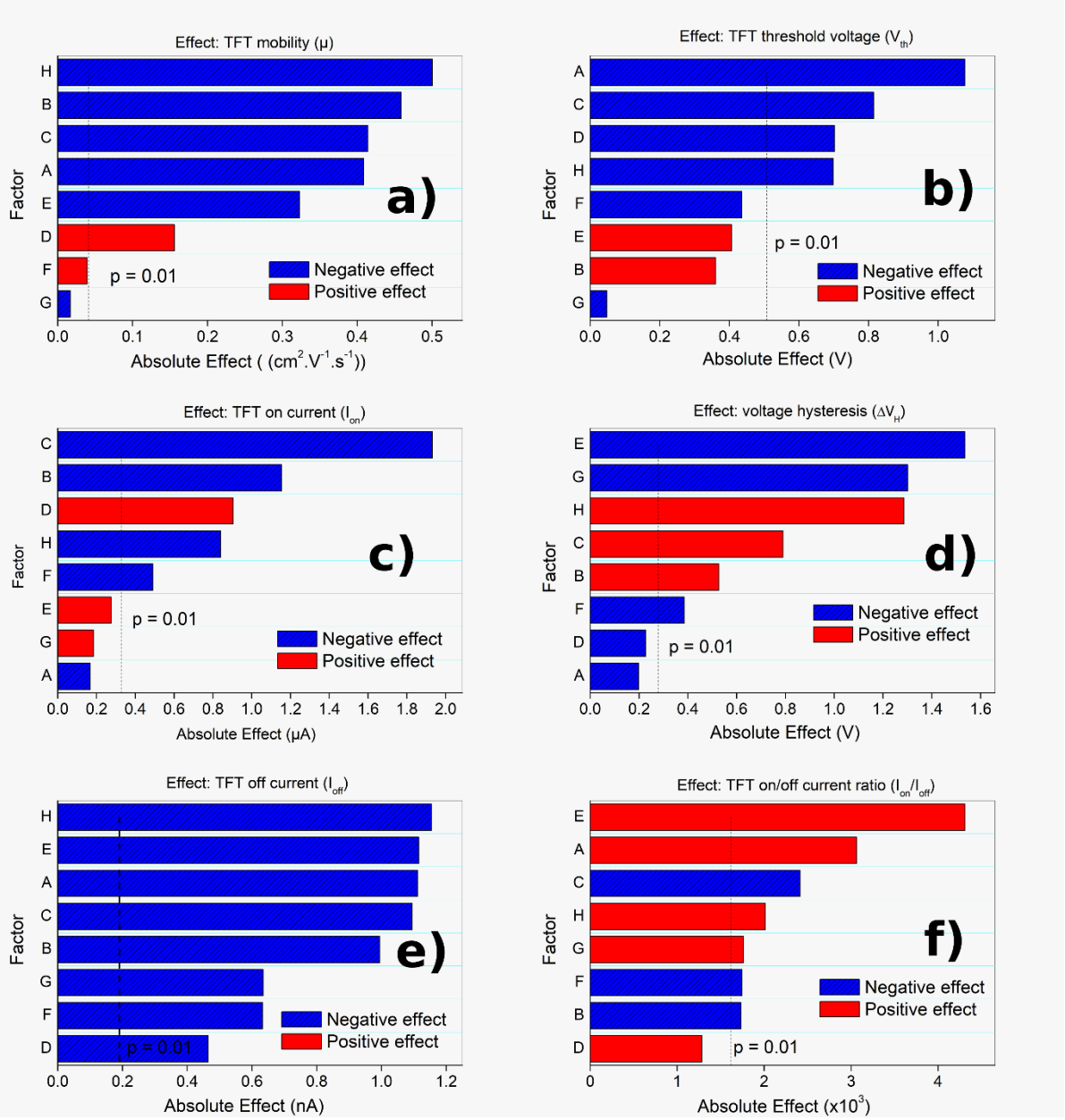


Figure 3: Pareto charts of the absolute effects on a) TFT mobility; b) TFT threshold voltage; c) voltage hysteresis; d) TFT "on" current; e) TFT "off" current; f) TFT on/off ratio.

The effect of a factor upon a response parameter is defined as positive (negative) if the response presents an absolute increase (decrease) by changing the factor level from "low" to "high". Colours are used to distinguish if the effect is negative or positive in the Pareto charts of Figure 3.

The Pareto charts show that several factors influence each response parameter considering a confidence interval of 99%. For the "off" current, all factors were found to be significant, whereas 7 factors were significant for both the mobility and the on/off ratio, 6 factors for the hysteresis, 5 factors for the "on" current and 4 factors for the threshold voltage. Moreover, the factors ranking and effect sign (positive or negative) change considerably among the observed responses. For improved factor screening, we considered only the factors which have a higher relative contribution to each response parameter, as described before during the analysis of Fig. 2. The results are presented in Table 4, where the percentage contribution and the cumulative contribution from the most significant factors are computed. Considering as relevant the factors which relative contribution to the effect is superior to 12.5%, we notice that a better screening of the manufacture factors (cells highlighted in yellow on Table 4). The exception is the threshold voltage, which have 4 significant factors and still have 4 relevant factors, summing up a cumulative contribution superior to 85%.

The anodization current density (factor F) is not among the most relevant factors in any of the cases, and the annealing treatment (factor G) and the electrolyte temperature (factor D) appear just once each among all cases, having smaller contributions to the observed effects. Table 4 also presents the sign of the influence of the factor (positive or negative) on the effect for each response, indicating the sign of the effect for a particular factor value ("high" or "low").

Table 4: Relative contribution to the effects and cumulative relative contribution from the manufacture factors considering the i) TFT mobility; ii) TFT threshold voltage; iii) voltage hysteresis; iv) TFT "on" current; v) TFT "off" current; vi) TFT on/off ratio as the response parameters.

Response: carrier mobility				
		Factor	Contribution (%)	Cumulative Contribution (%)
-	y	H	26.93	26.93
-	y	B	22.63	49.56
-	y	C	18.45	68.01
-	y	A	17.97	85.98
-	y	E	11.21	97.19
+	y	D	2.61	99.81
+	n	F	0.16	99.97
-	n	G	0.03	100.00

Response: threshold voltage				
		Factor	Contribution (%)	Cumulative Contribution (%)
-	y	A	35.26	35.26
-	y	C	20.17	55.42
-	y	D	14.98	70.40
-	y	H	14.80	85.21
-	n	F	5.76	90.97
+	n	E	5.02	95.98
+	n	B	3.95	99.93
-	n	G	0.07	100.00

Response: TFT channel "on" current				
		Factor	Contribution (%)	Cumulative Contribution (%)
-	y	C	53.59	53.59
-	y	B	19.12	72.71
+	y	D	11.72	84.44
-	y	H	10.13	94.56
-	y	F	3.46	98.02
+	n	E	1.09	99.11
+	n	G	0.49	99.60
-	n	A	0.40	100.00

Response: TFT channel "off" current				
		Factor	Contribution (%)	Cumulative Contribution (%)
-	y	H	18.97	18.97
-	y	E	17.72	36.70
-	y	A	17.62	54.31
-	y	C	17.08	71.39
-	y	B	14.09	85.48
-	y	G	5.74	91.21
-	y	F	5.71	96.92
-	y	D	3.08	100.00

Response: TFT on/off ratio				
		Factor	Contribution (%)	Cumulative Contribution (%)
+	y	E	38.17	38.17
+	y	A	19.30	57.47
-	y	C	11.98	69.45
+	y	H	8.35	77.80
+	y	G	6.38	84.18
-	y	F	6.27	90.45
-	y	B	6.16	96.62
+	n	D	3.38	100.00

Response: transfer curve hysteresis				
		Factor	Contribution (%)	Cumulative Contribution (%)
-	y	E	34.44	34.44
-	y	G	24.75	59.20
+	y	H	24.14	83.34
+	y	C	9.11	92.45
+	y	B	4.05	96.50
-	y	F	2.17	98.67
-	n	D	0.75	99.43
-	n	A	0.57	100.00

+	positive effect	A: Thickness of Al-layer	E: pH of the electrolyte
-	negative effect	B: Al-evaporation rate	F: Current density
y	significant fator	C: Water content	G: Annealing
n	non-significant factor	D: Temperature of electrolyte	H: Final voltage
	contribution > 12.5%		

The final voltage (H) is directly associated to the thickness of the Al_2O_3 and it is expected that, the higher the thickness, the lower the TFT mobility, "on" current and "off" current due to the lower electric field at the semiconductor/dielectric interface; this is supported by the data obtained in Table 4.

Conduction in the TFT channel initiates when the electric field at the interface induces the filling of gap states, moving the Fermi level closer to the conduction band and increasing the charge carrier concentration. Therefore, for voltages below V_{th}, most of the charge carriers are in localized states and the transport is dominated by hopping, which results in low mobility values [29]. The threshold voltage itself is mainly influenced by the presence of shallow states in the band gap, which are affected by the thickness of the dielectric layer and the oxide dielectric constant. Moreover, the higher density of traps resulting from a thicker dielectric layer can be also responsible for the observed higher transfer curve hysteresis.

The water content (C) in the electrolyte causes a higher Al_2O_3 surface roughness (see supplementary material, SI), which causes more carrier scattering at the dielectric interface, leading to lower mobility as well as "on" current and "off" current. The lower threshold voltage for higher water content may be because most of the defects formed in the dielectric layer are due to dipoles and not to charged states.

Hickmott [33] reported that the maximum amount of charges introduced into the Al_2O_3 layer during the anodization process can be more than 100 times larger when aqueous electrolytes are used. The effect of H_2O content in the electrolyte can be explained considering the equations used to describe the Al_2O_3 growth onto metallic Al:

$$2Al + 3/2\, O_2 \rightarrow Al_2O_3 \quad (2)$$

$$2Al + 3H_2O \rightarrow Al_2O_3 + 3H_2 \quad (3)$$

Whilst water residue is likely to be present on the surface, some water molecules or oxygen atoms can also be trapped in the Al_2O_3 bulk, creating defects which affect the electrical properties of the oxide layer, as well as the oxide surface roughness[34–36].

The Al-layer thickness (A) and the Al-evaporation rate (B) are also factors which affect the anodised oxide layer morphology [37] and conductivity (see SI) in such a way that the higher these factors, the lower are the TFT mobility and "on" current (higher carrier scattering at the interface) and the "off" current (lower channel intrinsic current, probably to defect states).

The data in table 4 also indicates that the pH of the electrolyte (E) impacts negatively the transfer curve hysteresis, denoting that for slower Al_2O_3 deposition rates (a more conductive electrolyte results in slower oxide growth), less charge traps are formed at the TFT semiconductor/dielectric interface. Hysteresis originates due to the delay on releasing charges from traps. During the forward sweep of V_G, traps with energy lower than the Fermi level are filled. During the reverse sweep, however, the charges are not released from the traps immediately, shifting the transfer curve compared to forward sweep. Therefore, interface states and traps in the bulk can be considered the main cause of hysteresis.

Factor E (pH of the electrolyte) is also the most important contribution to the TFT on/off ratio. Considering that both the "on" and "off" currents are negatively affected by the pH of the electrolyte, one concludes that the decrease on the "off" current is higher than the decrease on the "on" current, causing an increase on the on/off ratio when the factor is at its "high" level. A similar reasoning can be applied to explain why factor A (Al-film thickness) has a positive impact on the on/off ratio, despite its negative impact on both the TFT "on" and "off" currents. Another factor which has a high negative contribution to the transfer curve hysteresis (and, consequently to the charge traps density) is the annealing of the Al_2O_3 films prior to the ZnO sputtering. The substrate annealing promotes the desorption of adsorbed species (molecular oxygen, moisture, etc.) to the dielectric layer surface which can cause charge trapping at the semiconductor/dielectric interface during transistor operation.

TFT overall performance

A useful purpose of this work would be to identify the impact of the process factors on the overall performance of the ZnO TFTs. To analyse the effects of the manufacturing process, it is necessary to identify targets for each response parameter. We considered that, for the mobility, the "on" current and the on/off ratio, the best response is the highest value as possible, whereas, for the threshold voltage, the "off" current and the hysteresis, the best response is the lowest as possible. Using this criterion, Table 5 has been constructed, where the most appropriate target level (only "H" or "L") was selected for each response.

Table 5: Optimal choice for the level of each manufacturing factor considering the individual responses and the overall optimized performance considering the six response parameters from the TFT transfer curve. Yellow cells with a "n" indicate that the factor influence can be neglected.

	FACTORS							
	A	B	C	D	E	F	G	H
RESPONSES								
Mobility	H	L	L	n	n	n	n	L
Threshold Voltage	L	n	H	H	n	n	n	H
On current	n	L	L	n	n	n	n	n
Off current	H	H	H	n	H	n	n	H
On/off ratio	H	n	n	n	H	n	n	n
hysteresis	n	n	n	n	L	n	H	L
Optimum value	H	L	H	H	H	n	H	L

For each TFT response parameter, as different process factors could potentially lead to an optimised response, a method to identify the optimal process factor was needed. Therefore, we considered as major criterion the highest number of occurrences of each target level, as observed, for instance, for factor A in Table 5 (3x "H" *vs.* 1x "L", resulting in a target level "H"). However, for factor H (final voltage), each target level occurs twice, requiring the use of a second criterion. We considered the highest sum of the percental contribution of factor H to each response parameter (which can be obtained from Table 4), resulting in a target level "L" for factor H. As result, the

factor levels have an optimal combination of transistor performance in the last row of Table 5. One observes that factor F (current density) does not contribute significantly to the overall TFT performance and can be ignored, even though ANOVA showed initially that it was significant for some response parameters.

The scores of the factors for all parameters studied, calculated by ANOVA, are summarised in Table 6. The lines of the table are organised by separating the manufacturing factors in three different groups: i) factors prior to the anodisation step (the Al layer thickness and evaporation rate); ii) factors directly associated to the anodisation process (H_2O content, temperature of the electrolyte, pH of the electrolytic solution, current density and final voltage), and iii) the post-processing factors: in this case just the "annealing" step. Each cell of the table representing a significant factor (based upon the 12.5% relative contribution stated before) contains a number which represents the ranking of the factor influence on the associated response parameter.

Table 6: Comparative table of the significance scores of process factors considering all studied response parameters. The number in each cell represents the order of significance found by ANOVA for the respective pair of factor and parameter. Only factors which presented relative contribution superior to 12.5% were considered.

PARAMETERS			μ	V_{th}	I_{on}	I_{off}	I_{on}/I_{off}	ΔV_H
I)	Thick Al layer	A	4	1		3	2	
	Al Evap. Rate	B	2		2	5		
II)	H_2O content	C	3	2	1	4		
	Temp.Electrolyte	D		3				
	pH Electrolyte	E				2	1	1
	Current density	F						
	Final voltage	H	1	4		1		3
III)	Annealing	G						2

I) Pre-anodisation factors II) anodisation factors III) post-anodisation factor		Negative factor
		Positive factor

From this table, it is possible to identify that factors F and G (current density and annealing, respectively) are the factors which have the lowest overall impact upon performance considering all TFT response parameters. On the other hand, factors A, C and H (Al-film thickness, H_2O content in the electrolyte and final voltage, respectively) are the factors which have the highest impact on the overall performance. To rank the factors which impact most the overall performance, we can consider two criteria: i) the number of times each factor appears as significant in Table 6; and ii) the lowest sum of the order of significance in each line of Table 6. According to the first criterion, factors A, C and H are tied. However, by the second criterion, factor H (final voltage) is the most relevant factor, since it has the lowest sum of the order of significance. Factors A and C are still tied by such criterion. Moreover, factor H affects most the TFT mobility, which is commonly attributed as the most important TFT performance parameter. Therefore, Table 6 can be used to determine which process factors are the most important to the device performance, and which ones have a lower effect or can be neglected, in the case of the need of a full factorial DOE (when the factors interactions play an important role in the response parameters).

CONCLUSIONS

A combinational, two-level DOE approach based on a Plackett-Burman design with reduced number (12) of experimental runs, was applied to the screen 8 anodisation parameters used in the manufacturing of the gate dielectric of ZnO TFTs. The use of six performance parameters of TFTs allows for the preliminary identification of the correlations between the manufacturing process parameters and the device characteristics. An important observation from the results is that the manufacturing parameters of the dielectric layer of the TFTs have a strong influence on the device performance parameters, presenting a comparable effect (or even higher) on the device

characteristics than the variation of the dielectric layer surface treatment parameters, which are commonly investigated in the literature. The use of several replicated samples (eight, for each experimental run) increased considerably the number of degrees of freedom used in the analysis of variance of the DOE results, impacting positively the confidence interval and minimising the influence of noise on the method. This procedure is particularly interesting for optimisation of other devices in printed/flexible electronics to improve the fabrication process and to speed up the development of new low-cost products.

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Supporting Information Available: [Anodisation process details, TFT curves and Plackett-Burman analysis of performance parameters related to the insulating properties of the dielectric layer of the transistors or in metal-insulator-metal (MIM) capacitors structures]. This material is available free of charge via the Internet at http://pubs.acs.org.

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